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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TRAN, BINH X	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 04/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/863,978	CLOTHIER ET AL.	
	Examiner	Art Unit	
	Binh X Tran	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31 and 54* is/are pending in the application.

4a) Of the above claim(s) *54* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15,17-27 and 29-30* is/are rejected.

7)☒ Claim(s) *16,28 and 31* is/are objected to.

8)☒ Claim(s) *1-31 and 54* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/11/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of Claim 54

1. In the amendment filed on 9-15-2003, the applicants indicate that claim 54 is withdrawn. The applicants also indicates that claim 54 is withdrawn in the first paragraph of the remark filed on the same day. However, in last paragraph (in the first page of the remark), the applicants wrote, "Claim 54 is hereby cancelled without prejudice or disclaimer". Therefore, it is unclear from the record whether applicants would like to withdraw or cancel claim 54. For purpose of examination, the examiner will assume that claim 54 is withdrawn.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 18 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In line 3 of claim 18, "wherein said dielectric base layers is stiffening wherein said layers are attached together by a dielectric layer" (emphasis added) is indefinite. In claim 17, the applicants disclose a single "dielectric base layer". However in claim 18, applicants indicates a plurality of dielectric base layers. It is also unclear what specific layers that applicants wish to refer as "said layers" since there are many different layers in the claim. Further, it is unclear whether "a dielectric layer" (in the phrase "attached

together by a dielectric layer") is the same as "base dielectric layer" or not, since the dielectric base layer from sub-structure #1 can attach together with another dielectric base layer from sub-structure #2 to form a new repetitive structure.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-3, 5, 7, 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Yano et al. (US 6,419,149).

Respect to claim 1 Yano discloses a structure having first and second surfaces comprising:

a carrier foil (1) forming a first surface;

an electrically conductive layer (2) on the surface of the carrier foil (Fig 7a);

a dielectric layer (i.e. photoresist layer 4) located on the electrically conductive layer (2), wherein the dielectric layer having circuitry feature (See Fig 7c-4d);

a plated metal conductive circuitry (3) located with the circuitry features (4a) wherein the plated metal conductive circuitry (3) is substantially flush/coplanar with and surrounded by the dielectric, wherein the plated metal conductive and dielectric layer co-plane forms the second surface (Fig 7d, col. 1 lines 49 to col. line 15);

Respect to claim 2, Yano discloses the circuitry features in the dielectric layer are formed completely through the dielectric layer (4) to the conductive layer. Respect to claims 3, 5, Yano discloses circuitry features (3) are copper (col. 1 lines 59-61). Respect to claim 7, Yano discloses that the carrier foil (1) comprises copper (col. 1 lines 53-55). Respect to claim 12, Yano discloses the cavity (4a) exist thru the dielectric (4) layer to the electrically conductive layer (2), wherein said cavity resides an electronic component (3) (See Fig 7d).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 3, 5-6, 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asai (US 6,240,636) in view of Schmidt (US 5,457,881).

Asai discloses a structure having first and second surface comprising:

a carrier foil (10);

an electrically conductive layer (1) on one of the major surface of the carrier foil;

a dielectric layer (2) having circuitry feature (3);

a metal conductive circuitry located the circuitry features (i.e., inner wiring pattern 3) wherein the metal conductive circuitry is substantially flush/coplanar with and surrounded by the dielectric (2) (Fig 1, col. 2-3).

Asai fails to disclose that the metal circuitry features are plated. Schmidt teaches the metal circuitry features are plated (col. 2 lines 41-51). It would have been obvious to one having ordinary skill in the art, at the time of invention, to modify Asai in view of Schmidt by having plated metal circuitry because this plating process is easy to control.

Respect to claim 3, Asai discloses the circuitry features in the dielectric layer (2) are formed short of the conductive layer (Fig 1). Respect to claim 5, Asai discloses the metal conductive circuitry (i.e., inner wiring pattern) comprises copper (col. 7 lines 17-20). Respect to claims 6, Asai discloses the dielectric layer (2) comprises an epoxy resin (col. 3 lines 16-20) or polyimide (col. 4 lines 41-42). Respect to claim 12, Asai discloses a cavity (i.e. via hole 5) exists through the dielectric layer (2) to the electricity conductive layer (1) wherein the cavity (via hole 5) resides an outer copper layer (6) (Fig 1, read on "the cavity resides an electronic component"). Respect to claim 13-14, Asai discloses the structure was attached together by a dielectric layer (4) (Fig 1, read on "stiffening dielectric. Respect claim 15, Asia teaches interconnecting layer (3) of a conductive metal circuitry to layer (6) of the conductive metal circuitry.

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yano in view of Hayashi (US 6,359,235).

Claim 4 differs from Yano by the specific value of circuitry width and spacing value. Hayashi discloses that the circuitry width and spacing values are result effective variables. Hayashi further discloses a circuit width of 20 μm (Note: 20 μm = 0.787 mil, read on applicants' range of 0.5-3 mil) and a spacing of 20μm (read on applicants' range of 0.5-1 mil, Col. 12 lines 11-20). The result effective variable is commonly

determined by routine experiment. The process of conducting routine experiments so as to produce an expected result is obvious to one of ordinary skill in the art. Hence, it would have been obvious to one having ordinary skill in the art, at the time of invention, to perform routine experiment to obtain an optimal width and spacing as an expected result.

9. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yano in view of Takayama et al. (US 5,977,783).

Respect to claim 8, Yano discloses the conductive layer comprises nickel. Yano fails to disclose that conductive layer comprises chromium. Takayama teaches one can either use nickel or chromium for conductive layer (col. 4 lines 51-59). It would have been obvious to one having ordinary skill in the art, at the time of invention, to modify Yano in view of Takayama by using chromium because equivalent and substitution of one for the other would produce an expected result.

10. Claims 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asai in view of Schmidt and further in view of Hayashi.

Respect to claims 9-10, Asai fails to disclose the flush metal conductive circuitry is covered with gold. However, Asai discloses a device with flush metal conductive circuitry. Hayashi discloses a flush metal circuitry (3) is covered or selectively covered with gold layer (4) (Fig 1E, col. 5 lines 35-45). It would have been obvious to one having ordinary skill in the art, at the time of invention, to modify Asai and Schmidt in view of Hayashi by covering a flush circuitry with a gold layer because this would decrease the resistance.

Respect to claim 11, Hayashi discloses a gold wire bond (4) exist between gold covered circuitry layer (3) and layer (1) of the structure (Fig 1E, read on "between gold covered circuitry and other component").

12. Claims 17, 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kataoka et al. (US 6,270,889) in view of Schmidt (US 5,457,881).

Respect to claim 17, Kataoka discloses a structure having a first and second surface comprising:

a base dielectric (6') (Fig 4);

a second dielectric layer (6) containing circuitry feature (8') (i.e. wiring pattern) located upon the base dielectric (6);

metal conductive circuitry feature (8') located within the circuitry feature wherein the metal conductive circuitry is substantially flush/coplanar with and surround by the second dielectric (6), wherein the metal circuitry feature (8')/dielectric (6) co-plane form at leas on major surface (interface between feature (8') and layer (6), See Fig 4).

Kataoka fails to disclose that the metal circuitry features are plated. Schmidt teaches the metal circuitry features are plated by controlling plating parameters (col. 2 lines 41-51). It would have been obvious to one having ordinary skill in the art, at the time of invention, to modify Kataoka in view of Schmidt by having plated metal circuitry because this plating process is easy to control.

Respect to claim 19, Kataoka teaches the metal conductive circuitry (wiring pattern) is made of copper (col. 8 lines 29-30). Respect to claims 20-21, Kataoka

discloses the dielectric circuitry-containing layer and the dielectric base comprises epoxy resin or polyimide resin (col. 7 lines 60-65).

13. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kataoka in view of Schmidt and further in view of Asai and Hayashi.

Respect to claim 18, Kataoka and Schmidt fail to disclose the structure comprises repetitive layers of sub-structure and it is attached together by a dielectric layer. Asai discloses the structure comprises repetitive layers and it is attached together by a dielectric layer (4). It would have been obvious to one having ordinary skill in the art, at the time of invention, to modify Kataoka in view of Asai by attaching repetitive layers of said structure together by using a dielectric layer because this would allow creating multi-layer interconnect.

Claim 18 also differs from Kataoka, Schmidt and Asai by the specific value of circuitry width and spacing value. This limitation has been discussed above in Hayashi reference.

14. Claims 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kataoka in view Schmidt and further in view of Hayashi (US 6,359,235).

Respect to claim 22, Kataoka and Schmidt fail to disclose the flush metal conductive circuitry is covered with gold. However, Kataoka discloses a device with flush metal conductive circuitry. Hayashi discloses a flush metal circuitry (3) is covered or selectively covered with gold layer (4) (Fig 1E, col. 5 lines 35-45). It would have been obvious to one having ordinary skill in the art, at the time of invention, to modify Kataoka

and Schmidt in view of Hayashi by covering a flush circuitry with a gold layer because this would decrease the resistance.

Respect to claim 23 Hayashi discloses a gold wire bond (4) exist between gold covered circuitry and layer (1) (Fig 1E, read on "attach exist ...other component").

15. Claims 24-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kataoka in view of Schmidt and further in view of Asai.

Respect to claim 24, Kataoka and Schmidt fail to disclose a cavity exist through the dielectric layer to the metal conductive layer wherein the cavity having an electronic component. Asai discloses a cavity (i.e. via hole 5) exists through the dielectric layer (2) to the electricity conductive layer (1) wherein the cavity (via hole 5) resides an outer copper layer (6) (Fig 1, read on "said cavity resides an electronic component"). It would have been obvious to one having ordinary skill in the art, at the time of invention to modify Kataoka and Schmidt in view of Asai by having a cavity through the dielectric layer to the metal conductive layer because this would allow creating multi-layer interconnect. Respect to claims 25-26 Asai discloses the structure comprises repetitive layers and it is attached together by stiffening dielectric layer (4). Respect to claim 27, Asai teaches to interconnect layer (3) to layer (6).

16. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kataoka in view of Hayashi.

Claims 29 differ from Kataoka by the specific value of circuitry width and spacing value. Hayashi discloses that the circuitry width and spacing values are result effective variables. Hayashi further discloses a circuit width of 20 μm (Note: 20 μm = 0.787 mil,

read on applicants' range of 0.5-3 mil) and a spacing of 20μm (read on applicants' range of 0.5-1 mil, Col. 12 lines 11-20). The result effective variable is commonly determined by routine experiment. The process of conducting routine experiments so as to produce an expected result is obvious to one of ordinary skill in the art. Hence, it would have been obvious to one having ordinary skill in the art, at the time of invention, to perform routine experiment to obtain an optimal width and spacing as an expected result.

17. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kataoka, Hayashi (US 6,359,235) further in view of Asai.

Respect to claim 30, Kataoka and Hayashi fail to disclose a cavity exist through the dielectric layer to the metal conductive layer wherein the cavity having an electronic component. Asai discloses a cavity (i.e. via hole 5) exists through the dielectric layer (2) to the electricity conductive layer (1) wherein the cavity (via hole 5) resides an outer copper layer (6) interconnect with the inner copper layer (Fig 1, read on "integrated circuit chip"). It would have been obvious to one having ordinary skill in the art, at the time of invention to modify Kataoka and Hayashi in view of Asai by having a cavity through the dielectric layer to the metal conductive layer because this would allow creating multi-layer interconnect.

Allowable Subject Matter

18. Claims 16, 28 and 31 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

19. The following is a statement of reasons for the indication of allowable subject matter: The cited prior arts fail to disclose either a structure comprises a flush metal conductive circuitry interconnects from one via to another via; or a flush metal conductive having a gold wire bond attach exists between gold covered circuitry and the integrated chip in conjunction with all other limitation.

Response to Arguments

20. Applicant's arguments with respect to claims 1-28 have been considered but are moot in view of the new ground(s) of rejection. The examiner raises a new ground of rejection for claims 1-28 because the applicants amended those claims. However, the examiner decides to use Kataoka and/or Asai as one of the reference for the new 35 USC 103 rejection because it still reads on claim limitations.

21. The applicants argue, "Kataoka and Asai each discloses structures in which a circuitry/dielectric plane is buried and does not form a major surface". The examiner disagrees. This argument is not commensurate with the scope of the claims. A buried or unexposed plane still has a surface/major surface. There is no limitation in the claim which excluding the structure to have buried or unexposed surface.

Respect to claims 29-30, the applicants argue, "the references taking as a whole or severally fail to teach a circuitry/dielectric co-plane form a major surface of an electronic structure". The examiner disagrees. Kataoka clearly discloses circuitry (3) and dielectric layer (2) co-plane and has a major surface (See Fig 1-2, i.e. the interface between layer 2, 3 and layer 4). The examiner clearly recognizes that this surface is a buried surface. There are two kinds of surfaces: expose and unexposed (buried)

surface. The co-plane and buried surface of Kataoka certainly read on the claim limitation.

Conclusion

22. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh X Tran whose telephone number is (571) 272-1469. The examiner can normally be reached on Monday-Thursday and every other Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine G Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Binh X. Tran

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER